UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Addr ss: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

AMC

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/467,675	12/21/99	LIOU	F 252103-4540

EXAMINER	
NADAV, O	
ART UNIT	**PAPER NUMBER**
2811	

MM91/0412

DANIEL R MCCLURE
THOMAS KAYDEN HORSTEMEYER
& RISLEY LLP SUITE 1500
100 GALLERIA PARKWAY NW
ATLANTA GA 30339

DATE MAILED: 04/12/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/467,675	Applicant(s) Liou et al.
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Mar 12, 2001* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-21* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-21* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (6,118,154) in view of Hu et al. (6,121,077).

Yamaguchi et al. teach in figure 22 an ESD protection structure having a silicon sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad 30 and a node 71 and the internal circuit electrically connected to the node (figure 19), comprising a silicon resistor 36 formed over an insulating oxide material layer 2, electrically coupled between the input pad 30 and the node 71, at least a single crystal silicon sided P/N junction diode 34 formed over the insulating material layer 2, wherein the diode is electrically coupled between one terminal of a corresponding power supply 32 and a node 71.

Yamaguchi et al. do not teach a silicon layer comprising monocrystalline silicon.

Hu et al. teach an ESD protection circuit having an SOI structure formed of monocrystalline silicon (column 1, line 27).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a silicon layer comprising monocrystalline silicon in Yamaguchi et al.'s device because it is conventional in the art to form ESD protection device having an SOI structure of monocrystalline silicon in order to improve the performance of the device, of which judicial notice may be taken.

Regarding claims 4 and 10, Yamaguchi et al. teach an input buffer 37 electrically coupled between the node and the internal circuit.

Regarding claims 7, 13 and 17, Yamaguchi et al. teach a diode comprising a MOS transistor formed over the insulating layer, wherein one of the source/drain regions electrically connects to a gate by a wire line.

Regarding claim 8, Yamaguchi et al. teach junction diodes comprising first and second diodes, electrically connected between the node and one terminal of a first and second power supply, respectively.

Regarding claim 9, Yamaguchi et al. teach in figure 10 an input resistor comprising a plurality of single resistors 64 formed over the insulating material layer, wherein each of the resistors is electrically coupled between the input pad and the node. It would have

been obvious to a person of ordinary skill in the art at the time the invention was made to use an input resistor comprising a plurality of single resistors in Yamaguchi et al.'s device in order to provide better protection for the device.

Regarding claim 14, Yamaguchi et al. teach in figure 22 first, second and third conductive layers 13, 14, 15 formed over the insulating layer and electrically connecting the resistor between the input and the integrated circuit and the diode to the integrated circuit, respectively.

Regarding claim 19, Yamaguchi et al. (figures 10 and 22, #11) and Hu et al. (figure 14) teach resistors isolated by an isolation structure.

Regarding claim 20, it is conventional to use STI as an isolation structure, of which judicial notice may be taken.

Response to Arguments

3. Applicant argues on page 6 that, in contrast to Yamaguchi et al., the present invention recites a diode formed directly on the insulation layer, wherein no gate oxide is involved.

Yamaguchi et al. teach in figure 22 a diode (P/N junction) formed directly on the insulation layer 2. The broad recitation of the claim does not preclude an oxide layer from being formed over the diode.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav, Ph.D.

April 11, 2001

William Mintel

William Mintel
Primary Examiner
Art Unit 2811